CLAIMS:

What is claimed is:

1. A method of testing data retention of memory; including:

writing first data to a first memory sub-group during a first time period;

writing second data to a second memory sub-group during a second time period subsequent to said first time period;

pausing for a predetermined time interval during a third time period subsequent to said second time period;

reading a first one of said first and second data during a fourth time period subsequent to said third time period;

reading a second one of said first and second data during a fifth time period subsequent to said fourth time period; and

comparing said first and second ones of read data to expected results to determine data retention capabilities of said first and second memory sub-groups.

- 2. The method as recited in Claim 1 wherein said first and second data are written in a checkerboard pattern.
- 3. The method as recited in Claim 1 wherein said time interval is about 0 seconds.
- 4. The method as recited in Claim 3 wherein said time interval is between about 500 ms and about 1 s.

5. The method as recited in Claim 1 further comprising:

writing third data to said first memory sub-group during a sixth time period subsequent to said fifth time period;

writing fourth data to said second memory sub-group during a seventh time period subsequent to said sixth time period;

pausing during an eighth time period subsequent to said seventh time period;

reading a first one of said third and fourth data during a ninth time period subsequent to said eighth time period;

reading a second one of said third and fourth data during a tenth time period subsequent to said ninth time period; and

comparing said first and second ones of read third and fourth data to expected results to further determine said data retention capabilities of said first and second memory sub-groups.

- 6. The method as recited in Claim 5 wherein said first and second data are written in a first pattern and said third and fourth data are written in a second pattern different from said first pattern.
- 7. The method as recited in Claim 6 wherein said second pattern is an inverse of said first pattern.
- 8. The method as recited in Claim 6 wherein said first pattern is a checkerboard pattern and said second pattern is an inverse checkerboard pattern.

- 9. A system for testing data retention of memory, comprising:
 - a plurality of memory controllers each associated with and configured to access at least one memory sub-group;
 - a test controller configured to enable said memory controllers to:

write to said associated memory sub-groups during a plurality of first time periods that are each distinct to one of said memory controllers,

pause for a predetermined time interval during a second time period that is subsequent to said first time periods, and

read from said associated memory sub-groups during a plurality of third time periods that are each distinct to one of said memory controllers and subsequent to said second time period; and

- a comparison device configured to compare data read from said memory sub-groups to expected results to determine data retention capabilities of said memory sub-groups.
- 10. The system as recited in Claim 9 wherein said plurality of memory controllers includes a plurality of built-in self-test (BIST) controllers.
- 11. The system as recited in Claim 9 wherein said plurality of memory controllers includes dedicated memory controllers each associated with and configured to access one of said memory sub-groups.
- 12. The system as recited in Claim 9 wherein said plurality of memory controllers includes shared memory controllers each associated with and configured to access at least two of said memory sub-groups.

- 13. The system as recited in Claim 9 wherein said test controller includes a test access port (TAP) controller.
- 14. The system as recited in Claim 9 wherein said test controller is configured to enable said memory controllers to write data to said associated memory sub-groups in a predetermined pattern.
- 15. The system as recited in Claim 9 wherein said predetermined time interval is about 0 seconds.
- 16. The system as recited in Claim 9 wherein said predetermined time interval ranges between about 500 ms and 1 s.
- 17. The system as recited in Claim 14 wherein said pattern is a checkerboard pattern.
- 18. The system as recited in Claim 9 wherein said test controller is configured to enable said memory controllers to write data to said associated memory sub-groups in a first pattern during said first time periods and in a second pattern during a plurality of fourth time periods that are each distinct to one of said memory controllers and subsequent to said third time periods.
- 19. The system as recited in Claim 18 wherein said second pattern is an inverse of said first pattern.
- 20. The system as recited in Claim 19 wherein said first pattern is a checkerboard pattern and said second pattern is an inverse checkerboard pattern.

- 21. The system as recited in Claim 9 wherein said system and said memory sub-groups are integral to a common chip.
- 22. An system for testing data retention of memory, comprising:

means for accessing sub-groups of memory;

means for controlling said accessing means to:

write data to said memory sub-groups during a plurality of distinct first time periods,

pause for a predetermined time interval during a second time period that is subsequent to said first time periods, and

read data from said memory sub-groups during a plurality of distinct third time periods that are subsequent to said second time period; and

means for comparing said read data to expected results to determine data retention capabilities of said memory sub-groups.

- 23. The system as recited in Claim 22 wherein said accessing means include dedicated accessing means configured to access one of said memory sub-groups.
- 24. The system as recited in Claim 22 wherein said accessing means include shared accessing means configured to access at least two of said memory sub-groups.
- 25. The system as recited in Claim 22 wherein said predetermined time interval is about 0 seconds.
- 26. The system as recited in Claim 22 wherein said controlling means are configured to enable said accessing means to write data to said memory sub-groups in a predetermined pattern.

- 27. The system as recited in Claim 26 wherein said pattern is a checkerboard pattern.
- 28. The system as recited in Claim 22 wherein said controlling means are configured to enable said accessing means to write data to said memory sub-groups in a first pattern during said first time periods and in a second pattern during a plurality of distinct fourth time periods that are subsequent to said third time periods.
- 29. The system as recited in Claim 28 wherein said second pattern is an inverse of said first pattern.
- 30. The system as recited in Claim 22 wherein said system and said memory sub-groups are integral to a common chip.